

REMARKS

Claims 1-22 are pending in the application.

Claims 11-22 are withdrawn from consideration.

Claims 1-10 are rejected.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph.

Claim 1 is rejected under 35 U.S.C. 102(e).

Claim 2 is rejected under 35 U.S.C. 103(a).

Claims 1, 3 and 7 are currently amended.

No new matter is added.

Claims 1-10 remain in the case for reconsideration and allowance.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

Examiner Telephone Interview

Applicants thank the Examiner for her time for the telephone interview on September 14, 2005. During this phone conversation, applicant's representative, Brian Wichner (Reg. No. 52359), and the Examiner discussed the interpretation of the elements of FIG. 1 of the reference Greco. The Examiner stated that she has interpreted the figure as broadly as possible to read on the methods of the claims. The applicants suggested that they will probably argue, in the Office Action response, that the optional additional metal levels and their respective intervening dielectric layers are not shown by Greco to compose a capacitor, but may be merely electrical conductors (wires) that are insulated from each other.

Further discussion entailed clarification of the 35 U.S.C. 112 rejections of claims 1 and 7.

Specification

The abstract has been amended to not compare the invention with the prior art.

Claim Rejections - 35 USC § 112

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The applicants respectfully traverse the rejections.

Claim 1 has been amended to correct errors regarding antecedence. The corrected antecedence includes the elements "dielectric layer" and "contact hole."

Claim 3 has been amended to delete the term "conductive". Claim 1 has also been amended to include "comprising a material" so that proper antecedence is now established for claim 3. Support for this claim and amendment can be found, among other locations, on page 12, line 31 of the Specification.

Claims 7 has been amended to replace "a higher etching rate than" with "an etch selectivity relative to." Support for this claim and amendment can be found, among other locations, on page 14, line 14-16 of the Specification.

Claims 2, 4-6 and 8-10 depend from claim 1 and inherently include all of the limitations of the base claim. Therefore, claims 2, 4-6 and 8-10 are allowable for their dependency and their own merits.

Withdrawal of the rejections for claims 1-10 is thus requested.

Claim Rejections - 35 USC § 102

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Greco, et al., hereinafter as "Greco" (U.S. 5,926,359) (as understood by the Examiner in view of the Rejection under 35 U.S.C. 112).

The applicants respectfully traverse the rejection.

Claim 1 recites a MIM capacitor that includes a lower electrode, a dielectric layer, and an upper electrode. The dielectric layer is between the upper electrode and the lower electrode. The capacitor further includes a first wiring layer that is below or at a same level as the lower electrode, and the first wiring layer contacts the upper electrode through a contact hole in the dielectric layer. The method of claim 1 also includes patterning the dielectric layer to form the contact hole through which the surface of the first wiring layer is exposed, and forming the upper electrode to contact the first wiring layer through the contact hole.

Greco fails, however, to show these elements of claim 1, as explained below.

Referring to Greco's FIG. 1, apparent contact holes may have been formed to create the vias 30 and 36. These vias are in dielectric layer 25 and 35, respectively. Greco only shows the vias 36 contacting a second level of interconnecting wiring 11 to a first level of interconnecting wiring 12 (in the left of the figure) and the second level of interconnecting wiring 11 to the surface layer 19 (in the right of the figure), which is part of an upper

electrode of the capacitor 20 (col. 2, lines 50-53). Also, Greco's first level of interconnecting wiring 12 is considered a lower electrode (col. 2, lines 54-55).

In contrast, claim 1 of the application recites that a wiring layer is below or at the same level as a lower electrode. But Greco's second level of interconnecting wiring 11 is clearly *above* the lower electrode 12 (as well as the upper electrode). Thus the second level of interconnecting wiring 11 does not qualify as a first wiring layer, as recited in claim 1.

In fact, the only possible element taught by Greco that could pass for a first wiring layer, which is below a lower electrode, are the optional additional metal levels, labeled, but not even shown, in FIG. 1. But even then the first wiring layer would *not be insulated from the lower electrode*, which is a condition recited in claim 1.

Thus, no matter what elements taught by Greco are considered to be elements recited in claim 1, the condition of claim 1 that requires that the first wiring layer, which is at or below the level of the lower electrode, to contact the upper electrode through a contact hole in the dielectric layer, which is between the upper and lower electrodes, cannot be satisfied.

Additionally, the method recited in claim 1, *patterning the dielectric layer to form the contact hole through which the surface of the first wiring layer is exposed*, is not shown by Greco. Referring to FIG. 1, Greco shows vias 25 and 35, which may have been formed in contact holes. If so, then none of these contact holes would have exposed a first wiring layer that is at or below a lower electrode. For example, contact holes of vias 36 would have exposed a lower electrode 12, not a wiring layer that is at or below a lower electrode. Likewise, Greco does not show what contact holes of vias 30 may expose, and thus Greco cannot anticipate this part of the claim.

Also, the method recited in claim 1, *forming the upper electrode to contact the first wiring layer through the contact hole*, is not shown by Greco. Referring to FIG. 1, for example, Greco does not show an upper electrode contacting a wiring layer through a contact hole. Greco *does* show an upper electrode 16 apparently contacting interconnection wiring 11 through a contact hole of vias 36. But the interconnection wiring is not at or below a lower electrode 12.

In other words, although Greco shows elements that are apparently upper and lower electrodes, dielectric layers, contact holes, and wiring layers, none of these elements read on all of the elements of claim 1.

For at least the reasons stated above, applicants request withdrawal of the rejection.

Claim Rejections - 35 U.S.C. § 103

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Greco, et al. (U.S. 5,926,359) in view of Morrow, et al., hereinafter "Morrow" (U.S. 6,479,391) (as understood by the examiner in view of the Rejection under 35 U.S.C. 112).

The applicants respectfully traverse the rejection.

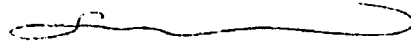
Claim 2 depends from claim 1 and inherently includes all of the limitations of the base claim. As discussed above, the prior art does not teach the limitations of the base claim much less the further embodiments of the dependent claims. Therefore, claim 2 is allowable for its dependency as well as its own merits. Allowance of this claim is requested.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-10 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

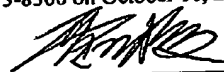
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